What is claimed is:

1. A method for selecting components for a matched set comprising the steps of:

electrically and mechanically coupling a semiconductor wafer having a plurality of integrated circuit chips to an interposer to form a wafer-interposer assembly;

testing the integrated circuit chips of the semiconductor wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies; and

selecting at least two of the chip assemblies for inclusion in the matched set based upon the testing.

2. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets.

3. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing groups of integrated circuit chips together to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized.

4. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify the compatibility of individual integrated circuit chips with one another.

5. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify which individual integrated circuit chips are incompatible with one another.

6. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for performance over a range of temperatures.

7. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises performing burn-in testing of the integrated circuit chips.

8. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises vibrating the integrated circuit chips.

9. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for leakage currents.

10. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for offset voltages.

11. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for gain tracking.

12. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for bandwidth.

13. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for speed grades.

14. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

15. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are analog devices.

16. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

17. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are mixed signal devices.

18. A method for assembling a matched set comprising the steps of:

providing a semiconductor wafer having a plurality of integrated circuit chips;

electrically and mechanically coupling the wafer to an interposer to form a wafer-interposer assembly;

testing the integrated circuit chips of the wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies;

sorting the chip assemblies based upon the testing; and

electrically coupling at least two of the chip assemblies onto a substrate, thereby assembling the matched set.

19. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets.

20. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing groups of integrated circuit chips together to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized.

21. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify the compatibility of individual integrated circuit chips with one another.

22. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify which individual integrated circuit chips are incompatible with one another.

23. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for performance over a range of temperatures.

24. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises performing burn-in testing of the integrated circuit chips.

25. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises vibrating the integrated circuit chips.

26. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for leakage currents.

27. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for offset voltages.

28. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for gain tracking.

29. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for bandwidth.

30. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for speed grades.

31. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

32. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer analog devices.

33. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer mixed signal devices.

34. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

35. A matched set assembled by the method as recited in claim 18.

36. A matched set of integrated circuit chips including at least two integrated circuit chips from wafer, the integrated circuit chips being tested together as part of a wafer-interposer assembly including the wafer and a wafer interposer, the matched set comprising:

a first chip assembly diced from the wafer-interposer assembly;

a second chip assembly diced from the wafer-interposer assembly; and

a substrate on to which the first and second chip assemblies are electrically coupled.

37. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

38. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are analog devices.

39. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

40. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are mixed signal devices.

41. The matched set as recited in claim 36 further comprising a third chip assembly diced from the wafer-interposer assembly, the third chip assembly electrically coupled to the substrate.